CLAIMS

What is claimed is:

1. A method comprising:

storing packet data within a storage element;

maintaining a transmit count value of said storage element;

determining a release count value of said storage element;

comparing said transmit count value and said release count value; and

de-allocating said storage element in response to comparing said transmit count value and said release count value.

2. The method of claim 1, further comprising:

receiving a packet including said packet data; and

allocating said storage element in response to receiving said packet.

3. The method of claim 1, further comprising transmitting said packet data from said storage element.

4. The method of claim 3, wherein maintaining a transmit count value of said storage element comprises:

initializing said transmit count value; and

incrementing said transmit count value by one in response to transmitting said packet data.

5. The method of claim 4, wherein comparing said transmit count value and said release count value comprises determining whether said incremented transmit count value

is equal to said release count value, and de-allocating said storage element in response to comparing said transmit count value and said release count value comprises de-allocating said storage element in response to a determination that said incremented transmit count value is equal to said release count value.

6. The method of claim 4, wherein transmitting said packet data from said storage element comprises transmitting said packet data from said storage element via a plurality of output interfaces.

7. The method of claim 6, wherein transmitting said packet data from said storage element via a plurality of output interfaces comprises transmitting said packet data from said storage element via a plurality of line interfaces.

8. The method of claim 7, wherein transmitting said packet data from said storage element via a plurality of line interfaces comprises transmitting said packet data from said storage element via a line interface selected from the group consisting of: an Ethernet interface, a Fast Ethernet interface, a Gigabit Ethernet interface, an OC-48/STM-16 interface, an OC-12/STM-14 interface, an OC-3/STM-1 interface, an IF Video interface, a DWDM interface, a DS-1 interface, a DS-3 interface, an E-1 interface, and an E-3 interface.

9. The method of claim 6, said packet data including a packet header and a packet body, wherein storing packet data within a storage element comprises:
storing said packet body within a common storage element; storing a copy of said packet header within a unique storage element for each of said plurality of output interfaces; and

associating each of said plurality of unique storage elements with said common storage element.

10. The method of claim 9, wherein initializing said transmit count value comprises setting said transmit count value of each of said plurality of unique storage elements equal to one less than said release count value.

11. An apparatus comprising:

an input module to store packet data within a storage element and to initialize a transmit count value of said storage element;

a processing element to determine a release count value of said storage element;

a direct memory access controller to transmit said packet data from said storage element; and

a memory controller to increment said transmit count value by one in response to a transmission of said packet data and to de-allocate said storage element in response to a determination that said incremented transmit count value is equal to said release count value.

12. The apparatus of claim 11, wherein said input module to store packet data within a storage element and to initialize a transmit count value of said storage element comprises an input module to receive a packet including said packet data and to allocate said storage element for said packet including said packet data.

13. The apparatus of claim 11, wherein said direct memory access controller to transmit said packet data from said storage element comprises a direct memory access

controller to transmit said packet data from said storage element via a plurality of output interfaces.

14. The apparatus of claim 13, wherein said direct memory access controller to transmit said packet data from said storage element via a plurality of output interfaces comprises a direct memory access controller to transmit said packet data from said storage element via a plurality of line interfaces.

15. The apparatus of claim 14, wherein said direct memory access controller to transmit said packet data from said storage element via a plurality of line interfaces comprises a direct memory access controller to transmit said packet data from said storage element via a line interface selected from the group consisting of: an Ethernet interface, a Fast Ethernet interface, a Gigabit Ethernet interface, an OC-48/STM-16 interface, an OC-12/STM-14 interface, an OC-3/STM-1 interface, an IF Video interface, a DWDM interface, a DS-1 interface, a DS-3 interface, an E-1 interface, and an E-3 interface.

16. The apparatus of claim 13, said packet data including a packet header and a packet body, wherein:

said input module to store packet data within a storage element and to initialize a transmit count value of said storage element comprises an input module to store said packet body within a common storage element; and

said processing element to determine a release count value of said storage element comprises a processing element to store a copy of said packet header within a unique

storage element for each of said plurality of output interfaces, and to associate each of said plurality of unique storage elements with said common storage element.

17. An apparatus comprising:

a first line card to transmit data to a communications network;

a line card interconnect coupled to said first line card; and

a second line card, coupled to said line card interconnect, to receive data from a communications network, said second line card including:

an input module to store packet data within a storage element and to initialize a transmit count value of said storage element;

a processing element to determine a release count value of said storage element;

a direct memory access controller to transmit said packet data from said storage element; and

a memory controller to increment said transmit count value by one in response to a transmission of said packet data and to de-allocate said storage element in response to a determination that said incremented transmit count value is equal to said release count value.

18. The apparatus of claim 17, said second line card further including a line interface module to receive data from a communications network, wherein said input module to store packet data within a storage element and to initialize a transmit count value of said storage element comprises an input module to receive a packet including said packet data from said line interface module and to allocate said storage element for said packet including said packet data.

19. The apparatus of claim 17, said second line card further including a memory, coupled to said memory controller, to store said a storage element.

20. The apparatus of claim 17, said second line card further including a line card interconnect interface module having a plurality of output interfaces coupled to said line card interconnect.

21. The apparatus of claim 20, wherein said direct memory access controller to transmit said packet data from said storage element comprises a direct memory access controller to transmit said packet data from said storage element to said line card interconnect interface module.

22. The apparatus of claim 20, wherein said direct memory access controller to transmit said packet data from said storage element comprises a direct memory access controller to transmit said packet data from said storage element via said plurality of output interfaces.

23. The apparatus of claim 22, said packet data including a packet header and a packet body, wherein:

said input module to store packet data within a storage element and to initialize a transmit count value of said storage element comprises an input module to store said packet body within a common storage element; and

said processing element to determine a release count value of said storage element comprises a processing element to store a copy of said packet header within a unique

storage element for each of said plurality of output interfaces, and to associate each of said plurality of unique storage elements with said common storage element.

24. An apparatus comprising:

a first line card to receive data from a communications network;

a line card interconnect coupled to said first line card; and

a second line card, coupled to said line card interconnect, to transmit data to a communications network, said second line card including:

an input module to store packet data within a storage element and to initialize a transmit count value of said storage element;

a processing element to determine a release count value of said storage element;

a direct memory access controller to transmit said packet data from said storage element; and

a memory controller to increment said transmit count value by one in response to a transmission of said packet data and to de-allocate said storage element in response to a determination that said incremented transmit count value is equal to said release count value.

25. The apparatus of claim 24, said second line card further including a line card interconnect interface module coupled to said line card interconnect, wherein said input module to store packet data within a storage element and to initialize a transmit count value of said storage element comprises an input module to receive a packet including said packet data from said line card interconnect interface module and to allocate said storage element for said packet including said packet data.

26. The apparatus of claim 24, said second line card further including a memory, coupled to said memory controller, to store said a storage element.

27. The apparatus of claim 24, said second line card further including a line interface module having a plurality of output interfaces.

28. The apparatus of claim 27, wherein said direct memory access controller to transmit said packet data from said storage element comprises a direct memory access controller to transmit said packet data from said storage element via said plurality of output interfaces.

29. The apparatus of claim 28, wherein said direct memory access controller to transmit said packet data from said storage element via said plurality of output interfaces comprises a direct memory access controller to transmit said packet data from said storage element via a line interface selected from the group consisting of: an Ethernet interface, a Fast Ethernet interface, a Gigabit Ethernet interface, an OC-48/STM-16 interface, an OC-12/STM-14 interface, an OC-3/STM-1 interface, an IF Video interface, a DWDM interface, a DS-1 interface, a DS-3 interface, an E-1 interface, and an E-3 interface.

30. The apparatus of claim 28, said packet data including a packet header and a packet body, wherein:

said input module to store packet data within a storage element and to initialize a transmit count value of said storage element comprises an input module to store said packet body within a common storage element; and

said processing element to determine a release count value of said storage element comprises a processing element to store a copy of said packet header within a unique storage element for each of said plurality of output interfaces, and to associate each of said plurality of unique storage elements with said common storage element.

31. A machine-readable medium that provides instructions, which when executed by a set of one or more processors, cause said set of processors to perform operations comprising:

storing packet data within a storage element;

maintaining a transmit count value of said storage element;

determining a release count value of said storage element;

comparing said transmit count value and said release count value; and

de-allocating said storage element in response to comparing said transmit count value and said release count value.

32. The machine-readable medium of claim 31, said operations further comprising:

receiving a packet including said packet data; and

allocating said storage element in response to receiving said packet.

33. The machine-readable medium of claim 31, said operations further comprising transmitting said packet data from said storage element.

34. The machine-readable medium of claim 33, wherein maintaining a transmit count value of said storage element comprises:

initializing said transmit count value; and

incrementing said transmit count value by one in response to transmitting said packet data.

35. The machine-readable medium of claim 34, wherein comparing said transmit count value and said release count value comprises determining whether said incremented transmit count value is equal to said release count value, and de-allocating said storage element in response to comparing said transmit count value and said release count value comprises de-allocating said storage element in response to a determination that said incremented transmit count value is equal to said release count value.

36. The machine-readable medium of claim 34, wherein transmitting said packet data from said storage element comprises transmitting said packet data from said storage element via a plurality of output interfaces.

37. The machine-readable medium of claim 36, wherein transmitting said packet data from said storage element via a plurality of output interfaces comprises transmitting said packet data from said storage element via a plurality of line interfaces.

38. The machine-readable medium of claim 37, wherein transmitting said packet data from said storage element via a plurality of line interfaces comprises transmitting said packet data from said storage element via a line interface selected from the group consisting of: an Ethernet interface, a Fast Ethernet interface, a Gigabit Ethernet interface, an OC-48/STM-16 interface, an OC-12/STM-14 interface, an OC-3/STM-1 interface, an IF Video interface, a DWDM interface, a DS-1 interface, a DS-3 interface, an E-1 interface, and an E-3 interface.

39. The machine-readable medium of claim 36, said packet data including a packet header and a packet body, wherein storing packet data within a storage element comprises:

storing said packet body within a common storage element;

storing a copy of said packet header within a unique storage element for each of said plurality of output interfaces; and

associating each of said plurality of unique storage elements with said common storage element.

40. The machine-readable medium of claim 39, wherein initializing said transmit count value comprises setting said transmit count value of each of said plurality of unique storage elements equal to one less than said release count value.